On Board Computer
Payload Data Handling Unit

PDHU

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November 2014
Avionics Overview for ULG
Advanced Data & Power Mgt System

The LEON processor board (unfolded)

ADPMS under test

1.5 Watt
300 gram
Avionics

November 2014
Avionics Overview for ULG
Avionics

- The Avionics Embedded System (AES) includes the hardware (processor, communication buses, equipments, instruments) and software required for the command & control of the spacecraft, its telecommand and telemetry handling, its failure detection, isolation and recovery and all the mission and vehicle management functions including all functional chains.

The AES is the brain of the spacecraft and therefore is a vital organ for the execution of onboard functions.

It represents today between 30 and 70 % of the platform non-recurrent development costs (50% in average for an ESA mission).
Avionics: Overview

- PCDU
- OBC
- OBSW
- CCSDS

Platform Equipments
- AOCS Sensors
- PWR System
- THERM System
- RF System
- ...

Payload Instruments
- Optical
- Scientific
- Telecom
- Radionavigation
- ...

Ground Segment

Spacelink
- Uplink (UL)
- Downlink (DL)

Telecommand (TC)
- Reception (Rx)

Telemetry (TM)
- Transmission (Tx)

Command (CMD)
- Control (CTRL)

Data (DAT)
Avionics: Overview (cont.)
Avionics: Hostile Environment

- **Temperature**: extreme conditions
  - Temperature range solar cells: -150 → +100 °C
  - Packaging, isolation and heaters: reduction to -20 → +50 °C
  - Commercial electronics don’t fit the bill: 0 → 70 °C
    (mil range -55 → +125 °C)

- **Ion radiation**: electron, proton, heavy ion (solar flare, van Allen belts)
  - Cumulated Effect:
    - Modification of the component characteristics
  - Single Event Effects:
    - SET: Single Event Transient (glitches) non destructive
    - SEU: Single Event Upset (swap) non destructive
    - SEL: Single Event Latchup (CMOS)
    - SEB: Single Event Burnout (MOSFET) destructive
    - SEGR: Single Event Gate Rupture destructive
Avionics: Protection Means

- **Radiation Protections**
  - Shielding
  - Box design
  - Positioning in the S/C
  - Technology choices
  - Build in electronic protection

- **Fault Tolerance**
  - Ability to support temporary or definitive modification or suppression of functionality
  - Redundancy
    - Processing: Spatial or Temporal Redundancy and Majority Voting
    - Duplicate the system: when a system is faulty, switch on the other one
    - Permit to eliminate the faulty system from the decision path (TMR technology)
    - Data Redundancy through coding, (RS, CRC, etc)
      - Error Detection and Correction (EDAC) on memory
      - Memory scrubbing to “clean” changed memory
OB Processor: Evolution

- **16 bits**
  - 2 MIPS
  - CPU Only
  - Mil Std

- **32 bits**
  - 14 MIPS
  - Sparc V7

- **32 bits**
  - 84 MIPS
  - Sparc V8
  - Cache

- **32 bits**
  - Pipe Line
  - Multi Core

- **128 bits**
  - 2 MIPS
  - CPU Only

- **128 bits**
  - 84 MIPS
  - Sparc V8
  - Cache

- **128 bits**
  - Pipe Line
  - Multi Core
Increase of the processor clock frequency is a method of achieving higher performance. This however leads to increase of processor power dissipation figure.

<table>
<thead>
<tr>
<th>Clock Speed of SPARC Architectures*</th>
<th>mid 90’s</th>
<th>end 90’s</th>
<th>mid 00’s</th>
</tr>
</thead>
<tbody>
<tr>
<td>ERC32 3-Chip Set</td>
<td>ERC32 Single Chip</td>
<td>LEON2-FT</td>
<td>AT697</td>
</tr>
<tr>
<td>ATMEL (TEMIC)</td>
<td>ATMEL (TEMIC)</td>
<td>ATMEL</td>
<td></td>
</tr>
<tr>
<td>0.8 mm</td>
<td>0.5 mm</td>
<td>0.18 mm</td>
<td></td>
</tr>
<tr>
<td>SPARC V7</td>
<td>SPARC V7</td>
<td>SPARC V8</td>
<td></td>
</tr>
<tr>
<td>10 MIPS 14 MHz</td>
<td>20 MIPS 25 MHz</td>
<td>85 MIPS</td>
<td>100 MHz</td>
</tr>
</tbody>
</table>

Extrapolating to 90 / 65 nm we obtain 250 / 400 MHz
Multi-core architecture is an alternative architectural solution that has the main advantage to increase the platform performance without increasing the power consumption.
Multi-processor architecture is yet another alternative architectural solution that allows for distributing the processing (e.g. image processing, complex gnc algorithms), on specialized, dedicated hardware (e.g. μp, dsp, fpga)
Processors vs Cores

- Processor
  - Memory
- Processor
  - Memory
- Processor
  - Memory

Bus Bottleneck Issue

- Core
  - Memory

- Core
  - Memory

- Core
  - Memory

Cache Coherency Issue

- Processor
  - Cache
  - Memory
- Processor
  - Cache
  - Memory
- Processor
  - Cache
  - Memory

- Core
  - Cache
  - Memory
- Core
  - Cache
  - Memory
- Core
  - Cache
  - Memory
SMP vs AMP

Symmetric Multi Processing

Supervised Asymmetric Multi Processing

Asymmetric Multi Processing
On Board Computer Memory

• Memory types
  
  • **PROM** (Programmable Read Only Memory)
    16 – 256 KB
    Board boot and init SW
  
  • **EEPROM** (Electrically Erasable Programmable Read Only Memory)
    2 – 8 MB
    the mission SW boot container, also used for safeguard
  
  • **SRAM** (Static Random Access Memory)
    4 – 16 MB;
    the workplace that contains executing SW and variables
  
  • **SDRAM** (Synchronous Dynamic Random Access Memory)
    16 to 512 MB
    slower RAM typically used for mass storage

- SRAM: data bit is stored in the state of a flip-flop (transistor logic - No power for Data Retention)
- DRAM: data bit is stored in the electric charge of a nano capacitor (Frequent Refresh Cycles, Volatile)
- MRAM: Magnetoresistive Random Access Memory (non-volatile magnetic storage)
- ROM: uses a metal mask to permanently enable/disable selected transistors instead of storing a charge in them
- FLASH: a kind of EEPROM erased and written in large blocks, read in a random access fashion (Non Volatile)
On Board Data Storage

- **Playing Tapes Storage** (Till 2000)
  - Mass Memory based on back and forward magnetic tapes.
  - Record in forward and play back in reverse (no time to rewind)
  - Robust to power failures

- **Solid State Mass Memory** (Nowadays)
  - Processor board can have 512 MB SDRAM Mass memory
  - Extra board could hold a GB (with battery back-up)
  - Very big Mass Memory units with almost unlimited size can be made in a very compact way (SDRAM or flash EPROM)
    - Interface through fast serial links (E.g. SpaceWire)
    - Mostly used for high resolution image satellites (e.g. 12 TB at EOL for Sentinel 2)
## On Board Communications Budget

<table>
<thead>
<tr>
<th>Flow (Proba 2)</th>
<th>From -&gt; To</th>
<th>Mbps</th>
</tr>
</thead>
<tbody>
<tr>
<td>TC segments</td>
<td>Ground → Spacecraft</td>
<td>2</td>
</tr>
<tr>
<td>TM/TC CLCW protocol feedback</td>
<td>TC/TM channels</td>
<td>0,01</td>
</tr>
<tr>
<td>TM Packets</td>
<td>TM → ground</td>
<td>2 x 66</td>
</tr>
<tr>
<td>AOCS control</td>
<td>OBSW → Eqts</td>
<td>0,1</td>
</tr>
<tr>
<td>AOCS telemetry</td>
<td>Eqts → OBSW</td>
<td>0,1</td>
</tr>
<tr>
<td>Payload control</td>
<td>OBSW → Payload</td>
<td>0,1</td>
</tr>
<tr>
<td>Payload Telemetry</td>
<td>Payload → OBSW</td>
<td>0,01</td>
</tr>
<tr>
<td>Spacecraft SW housekeeping</td>
<td>Eqts → OBSW</td>
<td>0,01</td>
</tr>
<tr>
<td>REM context writing</td>
<td>OBSW → REM</td>
<td>0,01</td>
</tr>
<tr>
<td>REM Watchdog kicking</td>
<td>REM → OBSW</td>
<td>0,01</td>
</tr>
<tr>
<td>PCM/PDM control</td>
<td>OBSW → PCM/PDM</td>
<td>0,01</td>
</tr>
<tr>
<td>PCM/PDM Telemetry</td>
<td>PCM/PDM → OBSW</td>
<td>0,01</td>
</tr>
<tr>
<td>Spacecraft HW housekeeping</td>
<td>Eqts → OBSW</td>
<td>0,01</td>
</tr>
<tr>
<td>REM housekeeping</td>
<td>REM (TM) → ground</td>
<td>0,01</td>
</tr>
<tr>
<td>Payload Data TM packets</td>
<td>Payload → TM</td>
<td>20</td>
</tr>
</tbody>
</table>
On Board Communication

On Board Communications

- Digital
  - Multi Drop Buses
    - Single Master
      - OBDH
      - Mil-Bus*
    - Multi Master
      - I2C
      - CanBus*
      - Spacewire*
  - Point-to-Point Links
    - Serial Line
    - Digital Converter
      - PacketWire
      - RS-422
      - RS-485
  - Analog
    - Point-to-point
      - Switchable Outputs
      - Statuses

Trade offs to be made:
- Power consumption
- Silicon surface, board surface
- Connectors and wiring harness (6 to 10% of weight of a satellite)
- Performance (throughput, response time)
- Isolation and fault propagation
- Intelligence required at slave end
- Required processing overhead

*may be redundant

Total harness weight (cables and connectors) may reach 6 to 10% of total satellite mass

On going studies investigate on board wireless communications
MilBus Basics

- From aircraft industry
- Mil-Std-1553-B Standard
- Multi Drop Bus
- Master/Slave
- Single cable
- Half Duplex
- Asynchronous
- Redundant (cross strapping)
- 1 Mbps (650 Kbps effective)
- Manchester Bi Phase Coding

1 Msg = 1 to 32 Words
1 Word = 16 Bits
Spacewire Basics

- High Speed Serial Link
- Fairly Simple
- High data rate (up to 400 Mbps)
- Low power consumption

- Promoted by ESA, based on IEEE 1533, DS Link, Transputer Technology
- Physical interface requires LVDS-tranceivers

- Packet based <Destination Address><Cargo><End_of_Packet>

- SpaceWire **Router** connects a number of SpaceWire link interfaces (receiver to transmitter ports)
- Group Adaptive Routing: group of links may be configure to increase throughput (bandwidth sharing) or fault tolerance
- Allow for different topologies following use needs
CAN Bus Basic

- Controller Area Network (CAN)
  - Automotive
  - Bosch / Intel
Ethernet Basics

- Deterministic Ethernet
  - AFDX
    (Avionics Full Duplex Switched Ethernet)
  - TT Ethernet
    (Time Triggered Ethernet)
Space Link Basic

- Radio Frequency
  - L-Band, S-Band, X-Band (Science Data)
  - Delay and Disruption Tolerant
  - Tracking and Ranging
  - Telecommand Uplink
  - Telemetry Downlink
TC Telecommands

- Receives TC bitstream from antenna/receiver
  - Hardware decoding of TC data streams:
    - Decoding bitstreams, error detection and correction, de-randomisation, overrun detection
    - Isolation of CLTU Command link Transmission Unit (which can contain several TC’s)
    - Generate FAR Frame Analysis Report for CLCW, send to TM module (COP-1 protocol)
  - Sends emergency TC’s directly to associated pulse generators
- Sending of TC’s to SW decoder
- Pulse generation (Pulse Distribution Unit)
  - Generates and distributes pulses without software intervention (reliability, precision)
TM Telemetry - Sources

- Sources of Telemetry allocated to separate VC Virtual Channels
  - Hardware generated TM’s:
    - Emergency telemetry: reporting of essential Telemetry: SW independent – low bandwidth <0.2 Kbps
    - Context memory (REM) dumps - < 6Kbps
  - Processor generated TM
    - Event driven TM’s, housekeeping, off-line and Mass Memory data... See SW design
  - TM from other sources (payloads, instruments) that inject directly TM without OBSW intervention
  - Idle packet generation: to keep the space link operational and synchronised if no real TM is available
- VCM (Virtual Channels Multiplexer):
  - Time multiplexes VC’s according to BAT (Bandwidth Allocation Table) on a per frame basis
Telemetry Encoder

- Handles the serialised TM frames:
  - Addition of Reed-Solomon Error Detection and Correction symbols
  - Pseudo-randomisation (to ensure bit transition density and avoid Tx DC components)
  - Optional Non-Return-to-Zero Mark encoding
  - Convolutional Encoding, such as Viterbi (doubles the bit rate)
  - Optional Split-Phase Level modulator (doubles bit rate)
  - Feed bitstream to radio amplifier/transmitter
OBC: System on Chip

- Saab Space, available in 2008 in Atmel ATC18RHA radiation hard 180 nm standard cell ASIC technology
- LEON2-FT Fault Tolerant SPARC V8 processor, 86 MIPS@100 MHz + FPU
- SPARC V8 Reference Memory Management Unit (MMU)
- Caches: 32 KB instruction, 16 KB data cache
- Extended Debug Support Unit (E-DSU) with 4096 trace lines
- EDAC and automatic scrubbing on large SDRAM, Memory Copy Controller
- 3 High-Speed UART’s
- Three MIL-STD-1553B bus interfaces
- OBDH bus Central Terminal
- 3 PacketWire Receivers & Transmitters
- 8 ECSS-E-50-12A SpaceWire Interfaces capable up to 200 MHz/160 Mbps, Hardware support for Remote Memory Access Protocol.
- 2 Controller Area Network (CAN) interfaces supporting up to 1 Mbps
Reconfiguration Module

• **Manages:**
  • The watchdog and associated computer reset and switch-over logic
  • The active and cold standby computer
  • The OBSW version to be loaded at start-up

• **It can as well contain:**
  • Context memory:
    • Serves as memory for time stamped logs of reconfiguration module, boot and application SW
    • Is not reset by a computer boot and regularly transferred to the ground.
  • Emergency TC hardware decoder and pulse generator
  • Central date and time system
OBP : LEON2

• Synthesisable Open Source VHDL model of a 32-bit SPARC V8
• Caches: 16 KB Data, 32 KB instructions
• Self standing computer: need only external clock and memory
• 2 timers + watchdog
• 2 UART, 32 parallel I/O
• Fault tolerant (parity, EDAC, TMR)
• Separate DSU (Debug Serial Unit) with normal serial line interface and transaction/instruction trace buffer with 512 entries
• Integrated PCI interface (50 % of chip)
• Virtual latchup free (70 MeV.cm$^2$/mg)
• Radiation up to 300 Krads (Si)

SPARC = Scalable Processor ARCHitecture = RISC (Reduced Instruction Set Computer) – 32 bit
RISC = Simple instruction set, simple CPU, target = 1 instruction per cycle (without memory R/W)
simple compiler, but needs 40 % bigger code size, better code optimisation
SUN SPARC strong points: One of the best performance & power figures per gate
SPARC architecture is no longer evolving but still holds up against other CPU designs
OBP: Dual Core LEON3

GR712RC Architecture © Aeroflex Gaisler AB
OBP: Quad Core LEON4

NGMP Architecture © Aeroflex Gaisler AB
Proba 1
- Centralized (star) architecture
  + Simple design, direct connection with the OBC
  + Well adapted to off the shelf equipment integration
- Modularity
- Harness

Mass:
- Structure 29kg
- Instruments 24kg
- Power 9.5kg
- AOCS 8.5kg
- Avionic & data processing 24kg
- RF 8kg
- Harness 12kg

Centralized (star) architecture

Simple design, direct connection with the OBC
Well adapted to off the shelf equipment integration
Modularity
Harness

Reaction Wheels (4)
Magnetometers (2)
Magnetotorquers (4)
GPS Receiver

AOCS I/F

PCS

Battery

Solar Array

SREM

DEBIE

PPU

CHRIS

Imagers

Other Payloads

Power line

Digital Control line
Bus architecture:
+ std protocol and communication schemes for all nodes
+ modularity/ testability
+ Bus traffic solved with central arbitration (CAN, 1553) or protocol arbitration (CAN, Ethernet)
- I/F component must be developed
- Bus redundancy
PROBA 2 Architecture

- Proba 2
- Internal busses (industrial standards)
- Main Boards/ generic communication (analog/digital I/Os, serial lines)
**Proba2: Main Facts & Figures**

**Processor board**
- 100MIPS
- 64 Mbyte SDRAM
- 4 Mbyte SRAM
- 4 Mbyte Flash
- 256 kBbyte Prom

**Mass memory**
- 4 Gbit
- with EDAC

**Context memory**
- 128 kbyte
- with EDAC

**Analogue Interfaces**
- Up to 80 analogue inputs
- Up to 32 temperature inputs

**Telecommand**
- 2 Mbps uplink capability
- 4 virtual channels or more
- configurable N° of MAP-ID
- 56 CPDU channels

**Telemetry**
- 100 Mbps downlink
- 5 virtual channels
- 2 packetwire inputs
- full encoding

**Communication Interfaces**
- Up to 25 UART channels
- Up to 6 TTC-B-01 channels
- a camera interface with frame grabber
- 2 packetwires

**Time interfaces**
- 8 programmable clock outputs
- 3 clock datation inputs

**Power distribution**
- 24 outputs of 28V / 50W
- current protected with auto restart
- switchable or non-switchable
- battery undervoltage protected with auto switch off

**Power conditioning**
- Up to 300W satellite peak power
- Up to 6 solar sections

**Centralised time synchronisation**

**Multi processor support**

**Backplane data throughput**
- up to 1 GBps

**Budgets:**
- Mass 13 kg
- Volume 455x160x267mm
- Power 17 W

**H/W generated emergency telemetry**

**H/W recovery TC decoder**

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Avionics : Proba 3

Commercial In Confidence

 Courtesy Verhaart Space
PROBA 3:

Commercial In Confidence

Courtesy Verhaert Space